IN THE CLAIMS

1-7 (Cancelled)

8. (Original) An apparatus, comprising:

a memory controller having a hardwired selection device to program the memory controller with a data mask mapping scheme, the data mask mapping scheme to associate at least one data mask bit with at least one data chunk in a memory module; and

an output to be coupled to the memory module.

9. (Original) The apparatus of claim 8, wherein the hardwired selection device is to receive the at least one data mask bit and at least a portion of the at least one data chunk.

10. (Original) The apparatus of claim 9, wherein the hardwired selection device is to select one of the at least one data mask bit to be associated with one of the at least one data chunk according to the data mask mapping scheme.

11. (Original) The apparatus of claim 8, wherein the hardwired selection device is to implement the data mask mapping scheme.

12. (Original) An apparatus, comprising:

a memory controller including a storage device having information to indicate a data mask mapping scheme for the memory controller; and

an output coupled to the memory module.

13. (Original) The apparatus of claim 12, wherein the storage device is loadable with the data mask map by software.

14. (Original) The apparatus of claim 12, wherein the storage device is loadable with the data mask map by BIOS.

15. (Original) The apparatus of claim 12, wherein the storage device is to include the information at manufacture time.

16. (Original) The apparatus of claim 12, wherein the information is to include at least one indicator to indicate the data mask mapping scheme.

17. (Original) The apparatus of claim 12, wherein the information is to include the data mask mapping scheme.

18. (Original) A system, comprising:

a memory module to use at least one data mask mapping scheme to associate at least one data mask bit with at least one data chunk;

a memory controller coupled with the memory module, the memory controller to be programmed with the at least one data mask mapping scheme used in the memory module.

19. (Original) The system of claim 18, wherein the memory module includes a first and a second memory rank to use at least one of the at least one data mask mapping scheme.

20. (Original) The system of claim 19, wherein the first memory rank is to use a different data mask mapping scheme than the second memory rank.

21. (Original) The system of claim 19, wherein the first memory rank is to use a same data mask mapping scheme as the second memory rank.

22. (Original) The system of claim 18, wherein the memory controller is to include a storage device to be programmed with one of the at least one data mask mapping scheme used in the memory module.

23. (Original) The system of claim 22, wherein the storage device is to be coupled with a selection device to select one of the at least one data mask bit to be associated with the at least one data chunk according to the data mask mapping scheme.

24-30 (Cancelled)